

Claims

1. A method for testing integrated circuit (IC) chips with probe needles on flat solder bumps comprising the steps of:

providing an IC chip with a multiplicity of bond pads on an active surface,

5 planting a multiplicity of solder bumps each having a height less than $\frac{1}{2}$ of its diameter on said multiplicity of bond pads, and

contacting said solder bumps with probe needles and establishing electrical connections with a test circuit.

2. A method for testing IC chips with probe needles on flat solder bumps according
10 to claim 1 further comprising the step of planting said multiplicity of solder bumps by a technique selected from the group consisting of evaporation, electroplating and molten solder screening.

3. A method for testing IC chips with probe needles on flat solder bumps according to claim 1 further comprising the step of planting said multiplicity of solder bumps each having a substantially flattened top surface.

4. A method for testing IC chips with probe needles on flat solder bumps according to claim 1 further comprising the steps of:

planting said multiplicity of solder bumps with a lead/tin solder material, and

planarizing said multiplicity of solder bumps forming a substantially flattened top

5 surface on each of said bumps.

5. A method for testing IC chips with probe needles on flat solder bumps according to claim 1 further comprising the steps of:

planting said multiplicity of solder bumps with a solder material containing at least 80% lead, and

10 flatten the top surfaces of said multiplicity of solder bumps by a platen having a planar surface.

6. A method for testing IC chips with probe needles on flat solder bumps according to claim 1 further comprising the step of planting said multiplicity of solder bumps by a molten solder screening transfer process, each of said multiplicity of solder bumps having a flattened

15 hemisphere.

7. A method for testing IC chips with probe needles on flat solder bumps according to claim 1 further comprising the step of planting said multiplicity of solder bumps by a molten solder screening technique in an in-situ mold such that each of the multiplicity of solder bumps planted has a flattened hemisphere.

8. A method for testing IC chips with probe needles on flat solder bumps according to claim 1 further comprising the steps of:

forming an in-situ solder mold on top of said IC chip with said multiplicity of solder bond pads exposed in a multiplicity of cavities,

5 filling said multiplicity of cavities with an electroplated solder material, and
removing said in-situ solder mold.

9. A method for testing IC chips with probe needles on flat solder bumps according to claim 8, wherein said in-situ solder mold is formed of a polymeric material.

10. 10. A method for testing IC chips with probe needles on flat solder bumps according to claim 8, wherein said in-situ solder mold is formed of a screen-printable polyimide material.

11. 11. A method for testing IC chips with probe needles on flat solder bumps according to claim 8, wherein said electroplated solder material filling said multiplicity of cavities forming short cylinders.

12. A method for testing IC chips with probe needles on flat solder bumps according to claim 1 further comprising the steps of:

forming an in-situ solder mold on top of said IC chip with said multiplicity of bond pads exposed in a multiplicity of cavities,

5 filling said multiplicity of cavities with a solder material by a molten solder screening technique, and

leaving said in-situ solder mold in place.

13. A method for testing IC chips with probe needles on flat solder bumps according to claim 12, wherein said in-situ mold is formed of a screen-printable polyimide material.

10 14. A method for testing IC chips with probe needles on flat solder bumps according to claim 12 further comprising the step of reflowing said solder material into solder balls for a final chip attach process.

15. An IC chip having substantially flattened solder bumps on an active surface comprising:

15 a multiplicity of bond pads formed on said active surface, and

a multiplicity of solder bumps formed in flattened hemi-spherical shape on said multiplicity of bond pads, each of said multiplicity of solder bumps having a height less than $\frac{1}{2}$ of the maximum diameter of said hemi-spherical shapes.

16. An IC chip having substantially flattened solder bumps on an active surface according to claim 15, wherein said multiplicity of solder bumps is formed of a lead-containing solder material.

5 17. An IC chip having substantially flattened solder bumps on an active surface according to claim 15, wherein said multiplicity of solder bumps is formed of a soft solder material and flattened on the top surfaces by a flat platen.

10 18. An IC chip having flat solder bumps on an active surface comprising:
 a multiplicity of bond pads formed on said active surface, and
 a multiplicity of solder bumps formed in cylindrical shape on said multiplicity of bond pads, each of said multiplicity of solder bumps having a height less than $\frac{1}{2}$ of the diameter of said cylindrical shape.

19. An IC chip having flat solder bumps on an active surface according to claim 18, wherein said multiplicity of solder bumps is formed of a lead-containing solder material.

15 20. An IC chip having flat solder bumps on an active surface according to claim 18, wherein said multiplicity of solder bumps is formed in a pancake shape.